UNITED STATES PATENT AND TRADEMARK OFFICE

MN

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/005,648	12/03/2001	Dale E. Gulick	2000.051600	8012

23720 7590 06/21/2007
WILLIAMS, MORGAN & AMERSON
10333 RICHMOND, SUITE 1100
HOUSTON, TX 77042

EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	
MAIL DATE	**DELIVERY MODE**
06/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/005,648
Filing Date: December 03, 2001
Appellant(s): GULICK, DALE E.

Mark W. Sincell, Ph.D.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12 February 2007 appealing from the Office action mailed 20 September 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The Examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

2002/0194415	LINDSAY	12-2002
6,516,398	HWANG	02-2003
6,182,235	MA et al.	01-2001
5,742,833	DEA et al.	04-1998
6,199,134	DESCHEPPER et al.	03-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-5, 9-22, 30, and 41-50 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Application Publication Number 2002/0194415 to Lindsay et al. ("Lindsay").

In reference to Claim 1, Lindsay discloses a microcontroller (See Figure 8 Number 825) configurable as either an Alert Standard Format master or an Alert Standard Format slave (See Paragraphs 12-15 and 86), wherein the microcontroller is configured as either the Alert Standard Format master or the Alert Standard Format slave (See

Paragraph 90), wherein the microcontroller is further configured as an Advanced Configuration and Power Interface controller (See Paragraphs 74, 75, 83, and 96).

In reference to Claim 2, Lindsay discloses the limitations as applied to Claim 1 above. Lindsay further discloses that the microcontroller is configured as the Alert Standard Format master (See Paragraph 90).

In reference to Claim 3, Lindsay discloses the limitations as applied to Claim 2 above. Lindsay further discloses that the microcontroller is coupled to an SMBus, and the microcontroller is further configured to receive Alert Standard Format status data from Alert Standard Format devices over the SMBus (See Paragraph 91).

In reference to Claim 4, Lindsay discloses the limitations as applied to Claim 1 above. Lindsay further discloses that the microcontroller is configured as the Alert Standard Format slave (See Paragraph 90).

In reference to Claim 5, Lindsay discloses the limitations as applied to Claim 4 above. Lindsay further discloses that the microcontroller is configured to receive status data from one or more Alert Standard Format devices, wherein the microcontroller is further configured to forward the status data from the one or more Alert Standard Format devices to the Alert Standard Format master (See Paragraph 92).

Claim 9 recites limitations that are substantially equivalent to those of Claim 1 and is rejected for the same reasoning as stated above.

Claim 10 recites limitations that are substantially equivalent to those of Claim 2 and is rejected for the same reasoning as stated above.

Claim 11 recites limitations that are substantially equivalent to those of Claim 3 and is rejected for the same reasoning as stated above.

In reference to Claim 12, Lindsay discloses the limitations as applied to Claim 10 above. Lindsay further discloses an Ethernet controller (See Figure 8 Number 808) coupled to the internal bus (See Figure 8 Number 811), wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus (See Paragraph 83).

In reference to Claim 13, Lindsay discloses the limitations as applied to Claim 12 above. Lindsay further discloses a plurality of buffers coupled between the microcontroller and the Ethernet controller for buffering the data (See Figure 8 Number 818 and Paragraph 83).

In reference to Claim 14, Lindsay discloses the limitations as applied to Claim 13 above. Lindsay further discloses that the plurality of buffers are connected between the

microcontroller and the Ethernet controller (See Figure 8 Number 818 and Paragraph 83).

In reference to Claim 15, Lindsay discloses the limitations as applied to Claim 12 above. Lindsay further discloses that the Ethernet controller is configured to route Alert Standard Format messages to the microcontroller (See Paragraphs 83 and 84).

In reference to Claim 16, Lindsay discloses the limitations as applied to Claim 12 above. Lindsay further discloses a remote management and control protocol set command unit connected to the internal bus, wherein the remote management and control protocol set command unit is configured to execute remote management and control protocol commands received from an external management server through the Ethernet controller. (See Paragraph 80).

Claim 17 recites limitations that are substantially equivalent to those of Claim 4 and is rejected for the same reasoning as stated above.

Claim 18 recites limitations that are substantially equivalent to those of Claim 5 and is rejected for the same reasoning as stated above.

In reference to Claim 19, Lindsay discloses the limitations as applied to Claim 17 above. Lindsay further discloses an Ethernet controller (See Figure 8 Number 808) coupled to

the internal bus (See Figure 8 Number 811), wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus (See Paragraph 83).

In reference to Claim 20, Lindsay discloses the limitations as applied to Claim 19 above. Lindsay further discloses a plurality of buffers coupled between the microcontroller and the Ethernet controller for buffering the data (See Figure 8 Number 818 and Paragraph 83).

In reference to Claim 21, Lindsay discloses the limitations as applied to Claim 20 above. Lindsay further discloses that the plurality of buffers are connected between the microcontroller and the Ethernet controller (See Figure 8 Number 818 and Paragraph 83).

In reference to Claim 22, Lindsay discloses the limitations as applied to Claim 19 above. Lindsay further discloses that the Ethernet controller is configured to route ASF messages to an external ASF master (See Paragraphs 83 and 84).

In reference to Claim 30, Lindsay discloses the limitations as applied to Claim 9 above. Lindsay further discloses that the integrated circuit further comprises an ASF status register (See Figure 8 Number 824).

In reference to Claim 41, Lindsay discloses an external bus (See Figure 8 Number 802); an integrated circuit, comprising: an internal bus (See Figure 8 Number 811); a microcontroller (See Figure 8 Number 825) configurable as either an Alert Standard Format master or an Alert Standard Format slave (See Paragraphs 12-15 and 86), wherein the microcontroller is configured as either the Alert Standard Format master or the Alert Standard Format slave (See Paragraph 90), wherein the microcontroller is further configured as an Advanced Configuration and Power Interface controller (See Paragraphs 74, 75, 83, and 96); and a bus interface logic connected to the external bus (See Figure 8 Number 806); and a processor coupled to the external bus.

In reference to Claim 42, Lindsay discloses the limitations as applied to Claim 41 above. Lindsay further discloses that the microcontroller is configured as the ASF master for the computer system (See Paragraph 90).

In reference to Claim 43, Lindsay discloses the limitations as applied to Claim 42 above. Lindsay further discloses an SMBus, one or more ASF devices coupled to the SMBus; and wherein the microcontroller is further configured to receive ASF status data from the one or more ASF devices over the SMBus (See Paragraph 91).

In reference to Claim 44, Lindsay discloses the limitations as applied to Claim 42 above. Lindsay further discloses an Ethernet controller (See Figure 8 Number 808) coupled to the internal bus (See Figure 8 Number 811), wherein the Ethernet controller and the

microcontroller are configured to exchange data over the internal bus (See Paragraph 83); and wherein the processor is configured to communicate over a network with the Ethernet controller (See Paragraphs 83).

In reference to Claim 45, Lindsay discloses the limitations as applied to Claim 44 above. Lindsay further discloses that the Ethernet controller is configured to route Alert Standard Format messages to the microcontroller (See Paragraphs 83 and 84).

In reference to Claim 46, Lindsay discloses the limitations as applied to Claim 44 above. Lindsay further discloses a remote management and control protocol set command unit connected to the internal bus, wherein the remote management and control protocol set command unit is configured to execute remote management and control protocol commands received from an external management server through the Ethernet controller. (See Paragraph 80).

In reference to Claim 47, Lindsay discloses the limitations as applied to Claim 41 above. Lindsay further discloses that the microcontroller is configured as the ASF slave (See Paragraph 90).

In reference to Claim 48, Lindsay discloses the limitations as applied to Claim 47 above. Lindsay further discloses that the microcontroller is configured to receive status data from one or more ASF devices, wherein the microcontroller is further configured to

forward the status data from the one or more ASF devices to a remote ASF master (See Paragraph 92).

In reference to Claim 49, Lindsay discloses the limitations as applied to Claim 48 above. Lindsay further discloses a network interface card coupled to the integrated circuit and to the processor, wherein the network interface card is configured as the Alert Standard Format master, and wherein the Ethernet controller is configured to route Alert Standard Format messages to the network interface card (See Figures 10 and 11).

In reference to Claim 50, Lindsay discloses the limitations as applied to Claim 47 above. Lindsay further discloses an Ethernet controller (See Figure 8 Number 808) coupled to the internal bus (See Figure 8 Number 811), wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus (See Paragraph 83).

Claims 6 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindsay as applied to Claims 1 and 9 above, and further in view of what was well known in the art as exemplified by any one of US Patent Number 6,516,398 to Hwang ("Hwang"), US Patent Number 6,182,235 Ma et al. ("Ma"), and US Patent Number 5,742,833 to Dea et al. ("Dea").

In reference to Claim 6, Lindsay teaches the limitations as applied to Claim 1 above. Lindsay does not teach that the microcontroller is further configured as an embedded 8051 microcontroller. The Examiner takes Official Notice that embedded 8051 microcontrollers are well known in the art for controlling a variety of devices, including appliances and computer devices, evidence of which may be found in: Hwang (See Column 1 Lines 27-44); Ma (See Column 1 Lines 11-31); and Dea (See Column 4 Lines 1-14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the use of an embedded 8051 microcontroller in the system of Lindsay, resulting in the invention of Claim 6, so as to take advantage of its widely recognized small size, low power consumption and versatility.

Claim 23 recites limitations that are substantially equivalent to those of Claim 6 and is rejected for the same reasoning as stated above.

Claims 7, 8, 24, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindsay as applied to Claims 1 and 9 above, and further in view of Applicant Admitted Prior Art ("AAPA").

In reference to Claims 7 and 8, Lindsay teaches the limitations as applied to Claim 1 above. Lindsay does not teach that the microcontroller is comprised in a bridge, as in

Claim 7, and that the bridge is a south bridge, as in Claim 8. AAPA teaches an integrated circuit configured as a south bridge (See Figure 1A Number 112).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to locate the microcontroller of Lindsay in the south bridge of AAPA, resulting in the inventions of Claims 7 and 8, because a south bridge provides an interface between various devices and subsystems and includes logic to interface with devices through the SMBus (See Page 3 Line 22 – Page 4 Line 4 of AAPA).

In reference to Claims 24 and 25, Lindsay teaches the limitations as applied to Claim 9 above. Lindsay does not teach that the integrated circuit is configured as a bridge, wherein the bridge further includes: a first bus interface logic for coupling to a first external bus; and a second bus interface logic for coupling to a second external bus, as in Claim 24, and that the bridge is configured as a south bridge, as in Claim 25. AAPA teaches an integrated circuit configured as a south bridge having first and second bus interface logic (See Figure 1A Number 112).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to locate the microcontroller of Lindsay in the south bridge of AAPA, resulting in the inventions of Claims 7 and 8, because a south bridge provides an interface between various devices and subsystems and includes logic to interface with devices through the SMBus (See Page 3 Line 22 – Page 4 Line 4 of AAPA).

In reference to Claim 26, Lindsay and AAPA teach the limitations as applied to Claim 25 above. Lindsay further teaches a plurality of registers and a register bridge connected to the internal bus, wherein the microcontroller is configured to read each of the plurality of south bridge registers through the register bridge (See Figure 8 Number 824).

Claims 27, 28, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindsay as applied to Claim 9 above, and further in view of US Patent Number 6,199,134 to Deschepper et al ("Deschepper").

In reference to Claims 27, 28, and 29, Lindsay teaches the limitations as applied to Claim 9 above. Lindsay does not teach a first embedded ACPI controller interface, as in Claim 27, a second embedded ACPI controller interface, as in Claim 28, and a third embedded ACPI controller interface, as in Claim 29. Deschepper teaches the use of embedded ACPI controller interfaces (See Abstract and Column 3 Line 55 – Column 4 Line 13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the microcontroller of Lindsay with the embedded ACPI controller interfaces of Deschepper, resulting in the inventions of Claims 27, 28, and 29, in order to allow components to be placed in a sleep mode to conserve power while still accurate data to be obtained from the component (See Column 3 Lines 18-30 and Column 4 Lines 49-65 of Deschepper).

Claims 55 and 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindsay, AAPA, and Deschepper.

In reference to Claim 55, Lindsay teaches receiving an Alert Standard Format message at a microcontroller (See Paragraphs 83 and 84). Lindsay further teaches that the device is an ACPI device (See Paragraphs 74, 75, 83, and 96). Lindsay does not teach receiving an ACPI event notification at the microcontroller; causing a system management interrupt to be generated using the microcontroller; and that the microcontroller is comprised in a south bridge. AAPA teaches an integrated circuit configured as a south bridge (See Figure 1A Number 112). Deschepper teaches a south bridge which receives an ACPI event notification and generates a system management interrupt (See Abstract and Column 3 Line 55 – Column 4 Line 13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to locate the microcontroller of Lindsay in the south bridge of AAPA using the ACPI events and SMI signals of Deschepper, resulting in the inventions of Claim 55, because a south bridge provides an interface between various devices and subsystems and includes logic to interface with devices through the SMBus (See Page 3 Line 22 – Page 4 Line 4 of AAPA) and to allow components to be placed in a sleep mode to conserve power while still accurate data to be obtained from the component (See Column 3 Lines 18-30 and Column 4 Lines 49-65 of Deschepper).

Claim 75 recites limitations that are substantially equivalent to those of Claim 55 and is rejected for the same reasoning as stated above.

(10) Response to Argument

In analyzing the claims, it is first necessary to determine the breadth of the claim language viewed in light of the disclosure. Any general purpose microcontroller can be configured for a variety of special purpose functions. It would be routine for one of ordinary skill in the art to select an appropriate microcontroller having appropriate capabilities to use in implementing a desired function. Appellant has provided no specific definitions of either an Alert Standard Format (ASF) master or an ASF slave, and thus one of ordinary skill in the art would look to the ASF specification as submitted by the Appellant. One of ordinary skill in the art would recognize that the claimed microcontroller configured as either an ASF master or an ASF slave is equivalent to a general purpose microcontroller programmed to function as either an ASF master or an ASF slave as defined by the ASF specification. Further, the claims do not require that the microcontroller be capable of configuration as both an ASF master and an ASF slave, but only require that it be capable of configuration as at least one or the other. Appellant has provided no specific definition of an Advanced Configuration Power Interface (ACPI) controller, and thus one of ordinary skill in the art would look to the ACPI specification and revisions as submitted by the Appellant. One of ordinary skill in the art would recognize that the claimed microcontroller configured as either an ACPI

controller is equivalent to a general purpose microcontroller programmed to function as an ACPI controller as defined by the ACPI specification.

Appellant has had ample opportunity to amend the claims to more clearly claim the subject matter sought to be distinguished over the prior art and has not done so. Thus, it is clear to the Examiner that Appellant intends to embrace the broadest possible interpretation of the claim language presented for consideration and thus the Examiner's interpretation of the breadth of the claim language is considered reasonable.

Appellant has argued that the controller of Lindsay is not configured as an Advanced Configuration and Power Interface controller (See Sections VII-B and VII-F). In response, the Examiner notes that Appellant has not explicitly defined an ACPI controller. One of ordinary skill in the art would thus interpret an ACPI controller in accordance with its broadest reasonable interpretations, which is any controller that performs operations in accordance with the ACPI protocol. Lindsay discloses that the devices depicted in Figures 7 and 8 are the same except for the integration of components into controller 825 (See Paragraph 83). Lindsay further discloses that the alerting network controller 918 is similar in functionality to controller 825 (See Paragraph 86). Controller 700, and likewise controller 800, are adapted to accommodate at least one protocol intended to effect management functionality (See Paragraph 74) which can be defined by the ACPI protocol (See Paragraph 75). The Examiner notes that it would be routine for one of ordinary skill in the art to configure a general purpose

microcontroller with programming to function as an ACPI controller as defined by the ACPI specification. Thus, the components of controllers 700 and 800 operate according to the ACPI protocol, and thus controller 825, which is a component of controller 800, is an ACPI controller.

Appellant has argued that Lindsay does not teach receiving an ACPI event notification in the ASF south bridge (See Section VII-F). In response, the Examiner notes that Lindsay was not relied upon to disclose this limitation. As shown in the above rejections regarding Claims 55 and 75, Deschepper was relied upon to disclose this limitation (See Abstract and Column 3 Line 55 – Column 4 Line 13).

Therefore, the Examiner believes that the Appellants arguments are not persuasive towards patentability.

Appellant has provided no new arguments with regard to Claims 6-8 and 23-29 (See Sections VII-C – VII-E) and relies solely upon the arguments presented with respect to their parent claims. As such, Claims 6-8 and 23-29 are considered to stand or fall with their parent claims.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the Examiner in the Related Appeals and Interferences section of this Examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Thomas J. Cleary
Patent Examiner
Art Unit 2111

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Conferees:

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100